February 1992
Revised April 2001

FAIRCHILD
SEMICONDUCTOR ™

74LVQ00
Low Voltage Quad 2-Input NAND Gate

General Description

The LVQ00 contains four 2-input NAND gates.

Features

■ Ideal for low power/low noise 3.3V applications
■ Guaranteed simultaneous switching noise level and dynamic threshold performance
■ Guaranteed pin-to-pin skew AC performance
■ Guaranteed incident wave switching into 75Ω

Ordering Code:

Order Number	Package Number	Package Description
74LVQ00SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LVQ00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
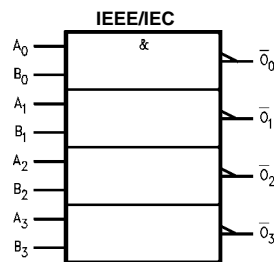
Connection Diagram
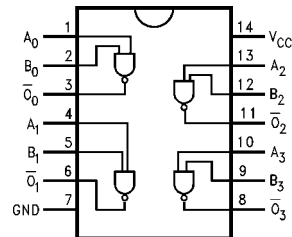
Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = +25°C$ Guaranteed Limits	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50$ μA
		3.0		2.58	2.48		$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA (Note 3)
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50$ μA
		3.0		0.36	0.44		$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA (Note 3)
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic Output Current (Note 4)	3.6			36	mA	$V_{OLD} = 0.8V$ Max (Note 5)
I_{OHD}		3.6			−25		$V_{OHD} = 2.0V$ Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0		V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−1.0		V	(Note 6)(Note 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0		V	(Note 6)(Note 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8		V	(Note 6)(Note 8)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

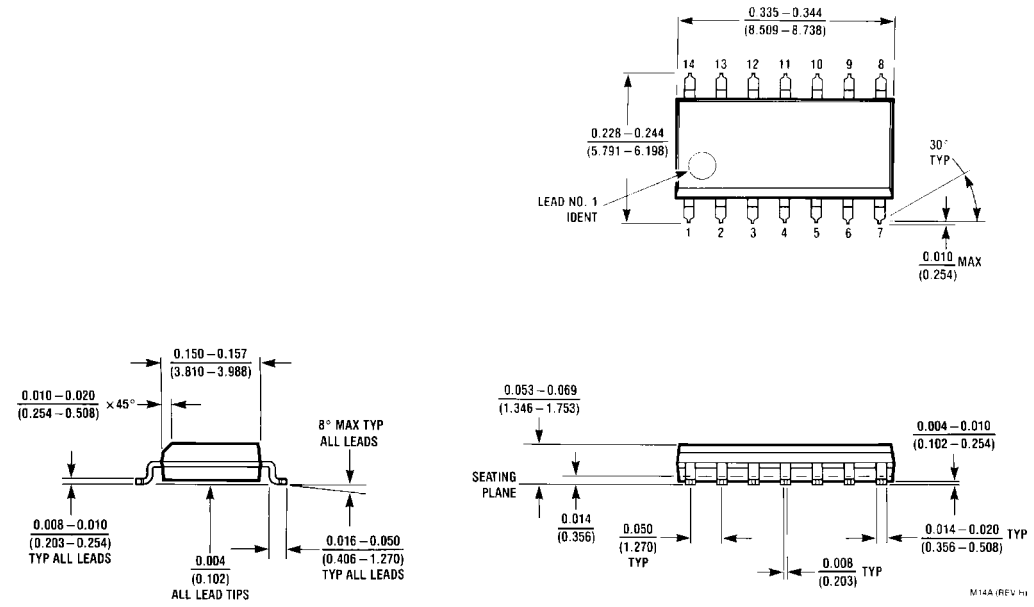| Symbol	Parameter	V_CC (V)	T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_PLH	Propagation Delay	2.7	2.0	8.4	13.4	2.0	14.0	ns
		3.3 ± 0.3	2.0	7.0	9.5	2.0	10.0	
t_PHL	Propagation Delay	2.7	1.5	6.6	11.3	1.0	12.0	ns
		3.3 ± 0.3	1.5	5.5	8.0	1.0	8.5	
t_OSHL,	Output to Output Skew	2.7		1.0	1.5		1.5	ns
t_OSLH	(Note 9)	3.3 ± 0.3		1.0	1.5		1.5	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_OSHL) or LOW-to-HIGH (t_OSLH). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_IN	Input Capacitance	4.5	pF	V_CC = Open
C_PD (Note 10)	Power Dissipation Capacitance	22	pF	V_CC = 3.3V

Note 10: C_PD is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted

$\dfrac{0.335 - 0.344}{(8.509 - 8.738)}$

14 13 12 11 10 9 8

$\dfrac{0.228 - 0.244}{(5.791 - 6.198)}$

30° TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

$\dfrac{0.010}{(0.254)}$ MAX

$\dfrac{0.150 - 0.157}{(3.810 - 3.988)}$

$\dfrac{0.010 - 0.020}{(0.254 - 0.508)} \times 45°$

8° MAX TYP
ALL LEADS

$\dfrac{0.008 - 0.010}{(0.203 - 0.254)}$ TYP ALL LEADS

$\dfrac{0.004}{(0.102)}$ ALL LEAD TIPS

$\dfrac{0.016 - 0.050}{(0.406 - 1.270)}$ TYP ALL LEADS

$\dfrac{0.053 - 0.069}{(1.346 - 1.753)}$

$\dfrac{0.004 - 0.010}{(0.102 - 0.254)}$

SEATING
PLANE

$\dfrac{0.014}{(0.356)}$

$\dfrac{0.050}{(1.270)}$ TYP

$\dfrac{0.008}{(0.203)}$ TYP

$\dfrac{0.014 - 0.020}{(0.356 - 0.508)}$ TYP

M14A (REV H)

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1
-A-

1.1 TYP

14   8

7.8

5.3±0.1
-B-

3.9

△ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.   1   7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.   △ 0.1 C   1.8±0.1

-C-

0.15±0.05

1.27 TYP   0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25
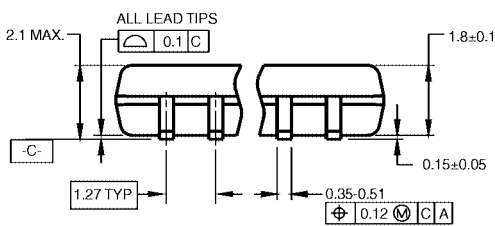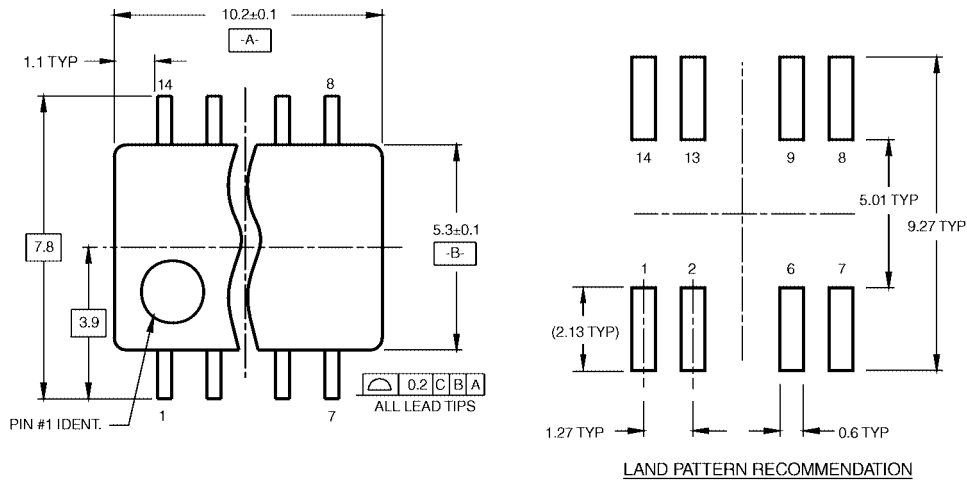
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

7° TYP

GAGE PLANE

0°-8° TYP   0.25

0.60±0.15   SEATING PLANE

1.25

DETAIL A
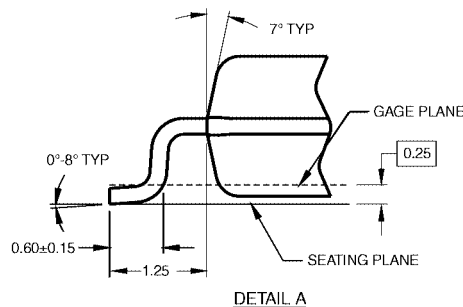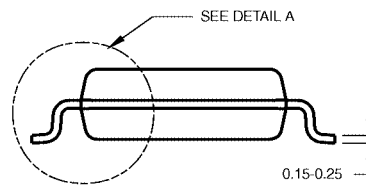
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com